METHOD AND APPARATUS FOR LOGIC LAYOUT WITH CONTROLLED PLACEMENT OF STRUCTURED CELLS

CROSS-REFERENCE TO RELATED APPLICATIONS

Not Applicable

STATEMET OF FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

This invention relates in general to integrated circuits and, more particularly, to a method and apparatus for electronic design automation.

2. DESCRIPTION OF THE RELATED ART

In the design of integrated circuits, a "place and route" tool is often used aid in the physical layout of a circuit. After the logic for a circuit is designed and tested, the cells of the circuit must be arranged in such a manner that desired timing (and other) constraints are met. A place and route tool can iterate

through different layouts and evaluate timing constraints for each layout until a suitable solution is reached.

As integrated circuits become denser, the layout of the circuit with respect to timing constraints becomes more critical and difficult. In a design that combines a large number of gates and aggressive timing criteria, it can be extremely difficult for a place and route tool to complete its task. In cases with many timing constraints, the place and route tool may not be able to complete all routes, as some constraints may be impossible to meet, or the number of iterations needed may be unacceptable.

Therefore, a need has arisen for a place and route system that allows flexible placement of critical paths to meet aggressive timing performances.

BRIEF SUMMARY OF THE INVENTION

In the present invention, an integrated circuit design includes datapath cells in a structured layout and other cells in an unstructured layout. A description of a desired layout for the datapath cells is generated and transferred to a place and route tool, in order to assign the desired layout to the datapath cells within the place and route tool. The datapath cells are assigned a predetermined status to prevent movement of the cells. Constraint information regarding the other cells is then transferred to the place and route tool and optimization procedures may be performed on the layout based on desired criteria, such that the datapaths cells are unmoved as different layout iterations are performed on the other cells.

The present invention provides several advantages over the prior art. The approach described above allows the layout designer to address both timing performance and density. Structured cells may be place in matrices that are not "hard macros"; therefore, they can be any shape that makes sense from a timing point of view. The placer can take advantage of the free space within matrices for improving density. Overall timing-driven placement is improved, since the place and route tool always has a global view of all timing constraints and can optimize the layout of no-fixed cell placements.